

Patent Claims

1. An amplifier comprising amplification means (AM) comprising an input and an output,
5 said amplification means (AM) comprising a switching output stage delivering at least one output signal (OUS) via said output,

said amplification means being fed by power supply means (PSM)

10 said amplifier further comprising compensation means (CM) providing a compensation signal (CS) derived from the power supply voltage (PSV) of the power supply means (PSM), said compensation signal (CS) comprising a substantially inverse representation of said power supply voltage (PSV) and

15 said compensation signal (CS) being fed to said amplification means (AM).
2. An amplifier according to claim 1, wherein said substantially inverse representation of the power supply voltage (PSV) is scaled by a ratio substantially corresponding to a desired amplification between the output and the input of the
20 amplification means (AM).
3. An amplifier according to claim 1 or claim 2, wherein said compensation signal is established for maintaining a substantially fixed utility area of a period of the amplified pulse width modulated signal regardless of changes in the power supply
25 voltage (PSV).
4. An amplifier according to any of the claims 1 to 3, wherein said compensation means further comprises extrapolation means (EM) adapted for modifying said compensation signal (CS) according to a predefined extrapolation algorithm.

5. An amplifier according to any of the claims 1 to 4, wherein said compensation signal (CS) is established on the basis of an inverting generator (CM) fed by a power supply comprising a circuit adapted for establishing an inverse signal of the voltage of said power supply.
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6. An amplifier according to any of the claims 1 to 5, wherein said inverting generator comprises at least one feedback loop having a power supply voltage dependent feedback.
- 10 7. An amplifier according to any of the claims 1 to 6, wherein said inverting generator comprises
at least one forward path (LF, MM, QM) having an input and an output,
at least one reference oscillator (SG)
at least one feedback path derived from said forward path and fed back to said input
15 of said forward path by means of a summing point (SP) subtracting the feed-back signal from an input received from said reference oscillator (SG)
wherein said feedback path comprises a power supply voltage dependent feedback
- 20 8. An amplifier according to any of the claims 1 to 7, wherein said inverting generator outputs a digital signal on the output (PWCS) of said forward path derived from at least one analog signal received in said input (PSVR).
- 25 9. An amplifier according to any of the claims 1 to 8, wherein said forward path comprises a limiter (MM) adapted for providing a pulse width modulated output signal (PWCS) of said forward path.
- 30 10. An amplifier according to any of the claims 1 to 9, wherein said forward path further comprises a time quantizer (QM) converting said pulse width modulated signal, preferably two level, into a time discrete signal fed to the output (PWCS) of said forward path.

11. An amplifier according to any of the claims 1 to 10, wherein said compensation signal is fed to said amplification means via at least one multiplication point (MP) in which the compensation signal is multiplied with a preferably digital input signal (IUS).
- 5 12. An amplifier according to any of the claims 1 to 11, wherein said compensation means further comprises decimation means (DM) adapted for transforming said compensation signal (CS) into compatibility with said input signal (IUS).
- 10 13. An amplifier according to any of the claims 1 to 12, wherein the signal processing performed by said amplification means multiplicatively depend on the power supply voltage.
14. An amplifier according to any of the claims 1 to 13, wherein said inverting
15 generator (CM) comprises at least one self-oscillating loop.
15. An amplifier according to any of the claims 1 to 14, wherein said self-oscillating loop comprises said at least one forward path (LF, MM, QM) and said at least one feedback path.
- 20 16. An amplifier according to any of the claims 1 to 15, wherein said forward path comprises at least one loop filter (LF).
17. An amplifier according to any of the claims 1 to 16, wherein said at least one
25 loop filter (LF) is adapted to facilitate self-oscillation.
18. An amplifier according to any of the claims 1 to 17, wherein the switch frequency of said pulse width modulated output signal (PWCS) provided by said limiter (MM) is at least partly defined by said at least one self-oscillating loop.
- 30 19. An amplifier according to any of the claims 1 to 18, wherein the order of said at least one loop filter (LF) is at least one.

20. An amplifier according to any of the claims 1 to 19, wherein the order of said at least one loop filter (LF) is at least two.
- 5 21. An amplifier according to any of the claims 1 to 20, wherein the effective order of said transfer function is at least one, preferably substantially two.
22. An amplifier according to any of the claims 1 to 21, wherein the phase margin (UPM) of the open loop characteristic of said self-oscillating loop for frequencies
10 within a frequency band starting from the upper limit of the utility band and ending at the switch frequency is between 0° and 60° , more preferably between 0° and 45° , and even more preferably between 0° and 30° .
23. An amplifier according to any of the claims 1 to 22, wherein said inverting
15 generator (CM) comprises switch frequency control means.
24. An amplifier according to any of the claims 1 to 23, wherein said switch frequency control means comprises an oscillating overlay signal generator connected to said at least one self-oscillating loop.
20
25. An amplifier according to any of the claims 1 to 24, wherein said reference oscillator (SG) provides a composite reference signal (RS) comprising a DC reference value and an oscillating overlay signal.
- 25 26. An amplifier according to any of the claims 1 to 25, wherein said oscillating overlay signal comprises a peak-to-peak amplitude of less than 10% of said DC reference value, preferably less than 5% of said DC reference value.
27. An amplifier according to any of the claims 1 to 26, wherein the clock frequency
30 of said time quantizer (QM) is at least ten times greater than said switch frequency, preferably at least hundred times greater.

28. An amplifier according to any of the claims 1 to 27, wherein said decimation means (DM) comprises an anti-aliasing filter having an impulse response which is longer than the period of said pulse width modulated output signal (PWCS), preferably at least the length of two times the period of said pulse width modulated output signal (PWCS), and even more preferably at least the length of three times the period of said pulse width modulated output signal (PWCS).

29. An amplifier according to any of the claims 1 to 28, wherein the stopband attenuation of said anti-aliasing filter of said decimation means (DM) is greater than 50dB, preferably greater than 70dB.

30. An amplifier according to any of the claims 1 to 29, wherein said anti-aliasing filter of said decimation means (DM) comprises stopbands defined by:

$$\text{Stopband} = k \cdot f_{\text{Sout}} \pm \text{BW},$$

where $k = 1, 2, 3, \dots$ until the Nyquist frequency is reached, f_{Sout} is the output rate of the decimation means (DM) and BW is the utility bandwidth, e.g. 20 kHz.

31. An amplifier according to any of the claims 1 to 30, wherein said anti-aliasing filter of said decimation means (DM) comprises at least two, preferably three, cascaded running average FIR filters.

32. An amplifier according claim 31, wherein said anti-aliasing filter of said decimation means (DM) further comprises two half-band FIR filters.

33. An amplifier according to any of the claims 1 to 32, wherein said power supply voltage dependent feedback comprises buffering means (BM).

34. An amplifier according to any of the claims 1 to 33, wherein said buffering means (BM) comprises certain specifications substantially representing corresponding specifications of said amplification means (AM).

35. An amplifier according to any of the claims 1 to 34, wherein said inverting generator is adapted for establishing at least one reciprocated electrical signal (PWCS), said inverting generator comprising at least one feedback loop, said at least one feedback loop comprising
- 5 at least one forward path being fed by a reference signal (RS) and comprising at least one non-linearity (MM), and
- at least one feedback path comprising at least one variable amplifier (BM), wherein at least one of said at least one variable amplifier is controlled on the basis of an electrical signal (PSVR).
- 10 36. An amplifier according to any of the claims 1 to 35, wherein at least one of said at least one feedback loop of said inverting generator comprises at least one quantization means (QM).
- 15 37. An amplifier according to any of the claims 1 to 36, wherein at least one of said at least one feedback loop of said inverting generator comprises at least one digital-to-analog conversion means (DAC).
38. An amplifier according to any of the claims 1 to 37, wherein at least one of said
- 20 at least one feedback loop of said inverting generator comprises at least one loop filter (LF).
39. An amplifier according to any of the claims 1 to 38, wherein at least one of said at least one forward path of said inverting generator comprises at least one analog-to-
- 25 digital converter (QM), preferably comprising at least one latch, and at least one of said at least one feedback path of said inverting generator comprises at least one digital-to-analog converter (DAC).
40. An amplifier according to any of the claims 1 to 39, wherein said input receives
- 30 at least one input signal (IUS, IUS1, IUS2, ... IUS6).

41. An amplifier according to any of the claims 1 to 40, wherein said input receives a composite signal, said composite signal comprises at least two input signals (IUS1, ISU2, ... IUS6).

5 42. An amplifier according to any of the claims 1 to 41, wherein said composite signal comprises two input signals, i.e. a stereo signal, six signals, i.e. a 5.1 surround sound signal, or eight signals, i.e. a 7.1 surround sound signal.

43. An amplifier according to any of the claims 1 to 42, wherein said amplification
10 means (AM) comprises at least one channel amplification means (AM1, AM2, ... AM6).

44. An amplifier according to any of the claims 1 to 43, wherein said amplification
15 means (AM) comprises two, five, six, seven or eight channel amplification means (AM1, AM2, ... AM6).

45. An amplifier according to any of the claims 1 to 44, wherein said amplification
20 means (AM) delivers one output signal, two output signals, five output signals, six output signals, or eight output signals (OUS, OUS1, OUS2, OUS6) via said output.

46. An amplifier according to any of the claims 1 to 45, wherein said compensation
25 signal (CS) is fed to at least one of said at least one channel amplification means (AM1, ... AM6) by multiplication with the corresponding said at least one input signal (IUS, IUS1, ... IUS6).

47. An amplifier according to any of the claims 1 to 46, wherein said extrapolation
means (EM) comprises distributed extrapolation means (EM1, ... EM6).

30 48. An amplifier according to any of the claims 1 to 47, wherein said compensation signal is fed to at least one of said at least one channel amplification means (AM1, ... AM6) by extrapolation by the corresponding said distributed extrapolation means

(EM1, ... EM6) and said multiplication with the corresponding said at least one input signal (IUS, IUS1, ... IUS6).

49. Method for compensating errors of a power signal (PS) comprising a power supply voltage (PSV), comprising the steps of

performing multiplicatively power supply voltage dependent signal processing on an input utility signal (IUS) by means of amplification means (AM),

10 establishing a compensation signal (CS) comprising a representation of the ratio between a desired voltage (DV) and said power supply voltage (PSV), and

applying said compensation signal (CS) to said input utility signal (IUS) by means of multiplication.

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50. Method for compensating errors of a power signal according to claim 49, whereby said establishment of a compensation signal (CS) comprises the steps of establishing a forward path fed by a reference signal (RS), establishing a negative feedback path from the output (PWCS) of said forward path,

20 and

scaling the signal of said feedback path proportionally with a representation (PSVR) of said power supply voltage (PSV).

51. Method for compensating errors of a power signal according to claim 49 or 50, whereby said establishment of a compensation signal (CS) comprises the steps of providing an electrical signal (PSVR), providing at least one feedback loop comprising

at least one forward path comprising at least one non-linearity (MM) and

at least one feedback path comprising at least one variable amplifier (BM),

30 feeding to at least one of said at least one variable amplifier said electrical signal (PSVR).

52. Method for compensating errors of a power signal according to any of the claims 49 to 51, whereby at least one of said at least one forward path is fed with at least one reference signal (RS).

5 53. Method for compensating errors of a power signal according to any of the claims 49 to 52, whereby at least one of said at least one feedback loop comprises at least one quantization means (QM).

10 54. Method for compensating errors of a power signal according to any of the claims 49 to 53, whereby at least one of said at least one feedback loop comprises at least one digital-to-analog conversion means (DAC).

15 55. Method for compensating errors of a power signal according to any of the claims 49 to 54, whereby quantization noise introduced by at least one of said at least one quantization means (QM) is shaped by at least one loop filter (LF).

56. Method for compensating errors of a power signal according to any of the claims 49 to 55, whereby said reference signal (RS) is an oscillating voltage signal.

20 57. Method for compensating errors of a power signal according to any of the claims 49 to 56, whereby said non-linearity (MM) is a limiter.

58. Method for compensating errors of a power signal according to any of the claims 49 to 57, whereby said non-linearity (MM) is a comparator.